AN INVESTIGATION OF GaAs MMIC HIGH POWER LIMITERS FOR CIRCUIT PROTECTION

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ABSTRACT

In this paper, we present an investigation of GaAs MMIC semiconductor limiters which can be fabricated on a standard MMIC process. This investigation, which included high power vector measurements of S-parameters over time, led to the design of a highly compact limiter integrated directly onto an FM-CW radar MMIC. As we demonstrate, the limiter significantly improved the lifetime of the FM-CW Radar MMIC when exposed to both single and multiple short, high power pulses of microwave energy.

INTRODUCTION

The protection of microwave circuits against high levels of incident power is best accomplished by the use of a limiter. A common limiter circuit topology involves the use of P-I-N diodes in shunt with the signal line [1]. Although these devices work very well as high power limiters, they are undesirable for MMIC applications since they cannot be fabricated on a standard GaAs process. In the past, limiters have been developed which can be fabricated on GaAs [2,3], but these limiters require a DC bias. Such a bias is not always available, especially if the limiter must protect a circuit when no DC power is applied.

Two GaAs semiconductor devices which exhibit limiting characteristics based upon their physics [4] without a DC bias are a semiconductor resistor in series with a signal line, and an enhancement mode MESFET (Efet) in shunt with a signal line. In this paper, we examine the limiting properties of a set of limiting elements. This investigation led to the development of a high power limiter integrated directly onto an FM-CW Radar MMIC [5]. The integrated limiter substantially improved the lifetime of the Radar MMIC when exposed to single and multiple pulses of short, high power microwave energy.

LIMITER CHARACTERIZATION

To quantify the limiting behavior of these devices, we first developed a custom high power test set for the high power measurement of two port devices. This test setup, shown in Figure 1, was designed for vector measurements of S11 (magnitude and angle) and scalar measurements of S12 (magnitude only) of a two port device-under-test (DUT). The variable attenuator provided a 20 dB range of input power, and two different traveling wave tube amplifiers (TWTs) were used to cover a range of incident powers from 26 to 53 dBm. This system was calibrated with a network analyzer to determine the losses between the crystal detectors and the connections to the TWT and the DUT. The calibration of the angle of S11 was accomplished with the two mixers and an open standard as the DUT. By driving the two mixers 90 degrees out of phase, we can uniquely determine the reflected angle from the expression:

$$\tan\phi = \frac{V_{90}}{V_0} \qquad (1)$$

where V_{90} and V_0 are the voltage outputs of the two mixers driven by the 90 and 0 degree outputs of the hybrid, respectively. We utilized a difference in path lengths to the two mixers to generate a 0 degree phase response for the open standard by slightly varying the transmit frequency. With our calibration techniques, this setup had a measurement

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accuracy of 1 dB in magnitude and 5 degrees in phase. In addition, the test set was designed to handle pulse widths of 50 ns and greater, and through software the setup could also deliver repeated pulses at a fixed incident power level to the DUT.

To quantify the limiting behavior of the series resistor and shunt Efet, we fabricated a series of two port test cells containing individual devices. As an example of our test capabilities, in Figure 2 we present the limiting characteristics of two devices, a 10 um x 250 um series depletion (D) resistor and a 100 um shunt Efet with two gate terminations. This measurement was made at each incident power level with a single 50 ns pulse, and we can clearly see the two devices have different limiting characteristics. In Figure 3, we demonstrate the vector capabilities of our setup by presenting the measurement of S11 over time (in polar form) during the failure pulse for a 100 um shunt Efet with its gate grounded. The incident power level was 34 dBm, and the pulse width was 5 us. We can clearly see in this figure that the device failed to a short (albeit not a perfect short) after 4 us of exposure.

Based upon this initial testing, we found that the series D-type semiconductor resistor limited over an 8 dB range of incident power, and the limiting turn-on point for the resistor was proportional to the square of the resistor width. For the shunt Efet with its gate grounded, the device limited for incident power levels above 30 dBm, whereas the open gate device limited above 38 dBm. These turn-on points were fairly independent of the total device periphery but dependent on the gate configuration. We also found the floating gate device had a higher survivability than the grounded gate device. Finally, we found that failure in these limiting elements was associated with a shorting of the semiconductor region.

LIMITER INTEGRATION

With the insight gained from our initial study, we next designed a limiter for high power protection of a 5.8 GHz FM-CW Radar MMIC used in ranging applications. The limiter was required to protect the MMIC against short, high power pulses without the need for DC power. In addition, the limiter could have no more than 1.5 dB insertion loss for power levels below +20 dBm. To satisfy these goals, we designed a shunt Efet - series D resistor limiter with a small signal insertion loss of 1.5 dB. A schematic of the limiter is shown in Figure 4. This limiter was integrated directly onto the FM-CW Radar MMIC and only required an area of 100 um x 300 um. A photograph of the radar MMIC die with the integrated limiter is shown in Figure 5.

EVALUATION OF INTEGRATED LIMITER

In Figure 6, we present the incident power level which caused device failure in a single pulse, with and without the integrated limiter, versus pulse width. The radar MMIC was encapsulated in an SOIC-8 package for this testing, and the results are averaged over 6 tests at each pulse width. The error bars represent one standard deviation in power at failure. We note that the integrated limiter improved the single pulse survivability of the MMIC to 100 W at a 100 ns pulse width, which was 8 dB higher than the MMIC without the limiter. In addition, we also examined the reliability of the MMIC in the SOIC-8 package when exposed to repeated pulses of sub-catastrophic power. This repeated lifetime study was carried out using a novel accelerated lifetime testing technique, where the incident energy level was used as the lifetime accelerant. We exposed a sample population of the MMICs to power levels below the single pulse thresholds and determined a mean number of pulses to failure. We discovered that the mean number of pulses to failure of both MMICs was dependent on the incident energy level through an Arrhenius-type relation [6] with a measurable activation energy:

$$MPTF = A\exp\left(E_A \big/ J_{inc}\right) \qquad (2)$$

where MPTF is the mean number of pulses to failure, J_{inc} is the incident energy of each pulse, E_A is the activation energy, and A is a constant. In Figure 7, we present the number of pulses to failure versus the incident energy for the two MMICs with and without an

integrated limiter. In addition, we present the curve fits of the mean data to Eq. (2), where the coefficients are described in Table 1.

MMIC	A	E_A (uJ)
with limiter	0.01	34.373
without limiter	1.41	2.605

Table 1. Coefficients for curve fits in Figure 7.

We can clearly see the integrated limiter MMIC has a much higher activation energy, which translates into a larger mean number of pulses to failure at a given level of incident energy when compared to the FM-CW Radar MMIC without a limiter.

CONCLUSIONS

The integration of a high power limiter onto a GaAs MMIC has been discussed in this paper. The limiter improved the survivability of the MMIC when exposed to a single, short, high power pulse of incident energy by 8 dB over the unprotected MMIC. In addition, the integrated limiter MMIC has a much longer lifetime than the unprotected MMIC when repeatedly exposed to short, high power pulses.

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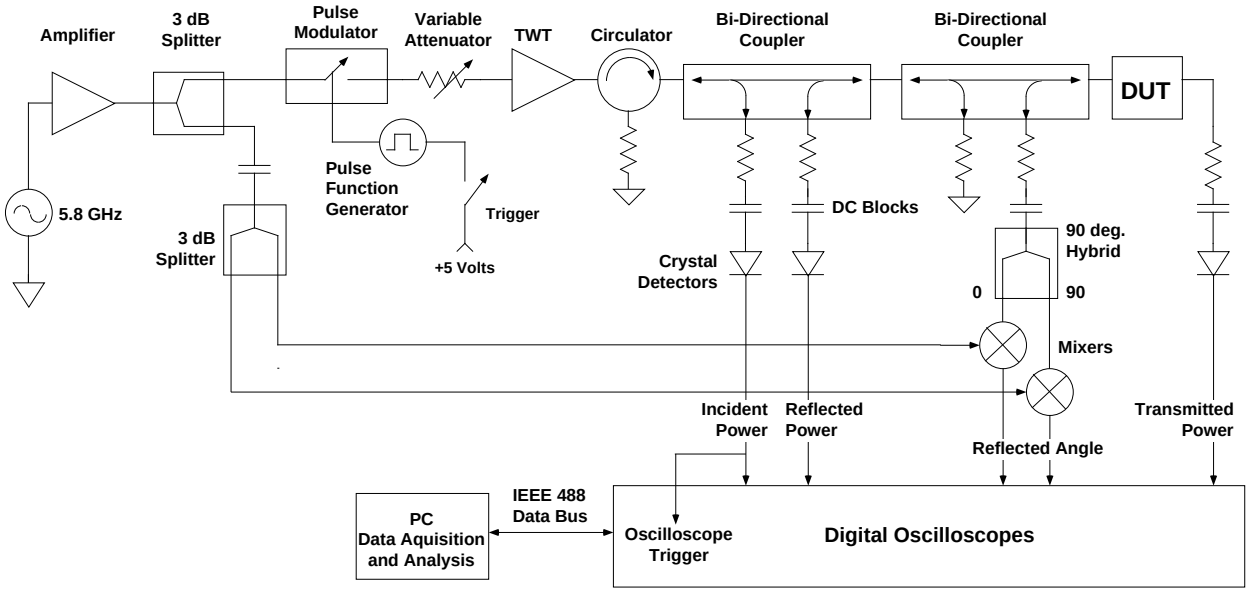

Figure 1. Schematic of the high power vector measurement setup.

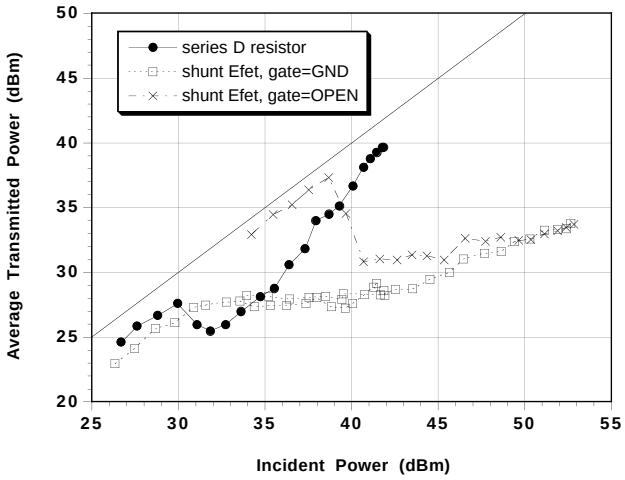

Figure 2. Limiting characteristics of series D resistor and shunt Efet. Pulse width = 50 ns.

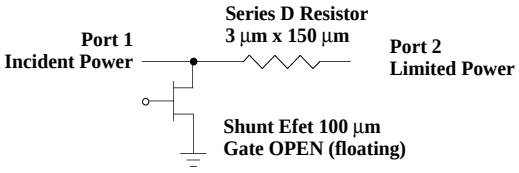

Figure 4. Schematic of limiter integrated onto FM-CW radar chip.

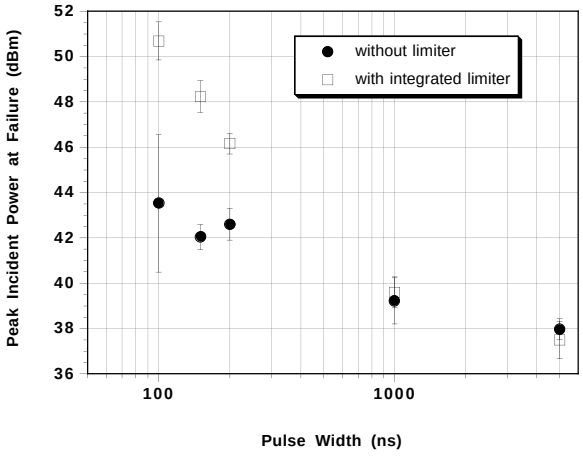

Figure 6. Summary of single pulse failure thresholds versus pulse width for FM-CW Radar MMIC.

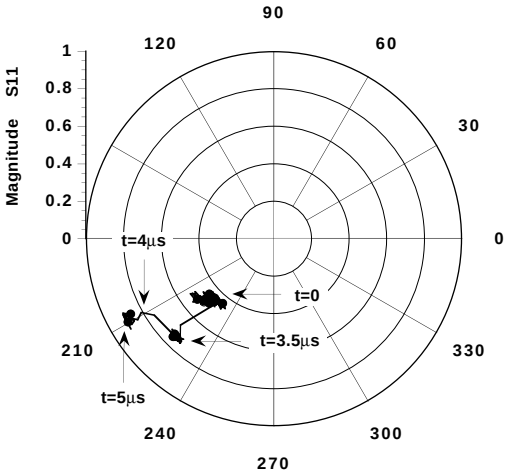

Figure 3. Measurement of S11 during single pulse failure for 100 um shunt Efet, gate grounded. Pulse width = 5 us, incident power = 34 dBm.

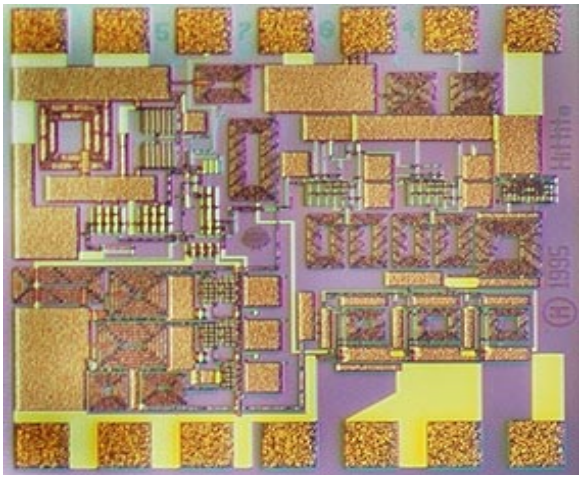

Figure 5. FM-CW radar chip with integrated limiter.

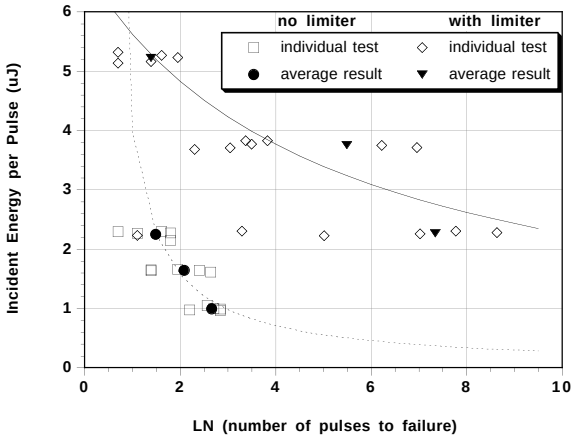

Figure 7. Mean number of pulses to failure versus incident energy for the FM-CW radar chip in SOIC-8 package with and without an integrated limiter.